
Peak pulse voltage ($T_j=25$; non-repetitive, off-state; FIG.8)	V_{pp}	4	kV
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ELECTRICAL CHARACTERISTICS ($T_j=25$ unless otherwise specified)

Symbol	Test Condition	Quadrant	Value		Unit
I_{GT}	$V_D=12V$ $R_L=33\Omega$	- -	MAX.	5	mA
V_{GT}		- -	MAX.	1	V
V_{GD}	$V_D=V_{DRM}$ $T_j=125$ $R_L=3.3k\Omega$	- -	MIN.	0.2	V
I_L	$I_G=1.2I_{GT}$	-	MAX.	10	mA
				15	
I_H	$I_T=100mA$		MAX.	10	mA
dV/dt	$V_D=400V$ Gate Open $T_j=125$		MIN.	150	V/ μs
$(dI/dt)_c$	$(dV/dt)_c=10V/\mu s$, $T_j=125$		MIN.	1	A/ms
t_{on}	$I_G=10mA$ $I_A=200mA$ $I_R=20mA$ $T_j=25$		TYP.	2	μs
t_{off}				20	

STATIC CHARACTERISTICS

Symbol	Parameter		Value(MAX.)	Unit
V_{TM}	$I_{TM}=1.5A$ $t_p=380\mu s$	$T_j=25$	1.35	V
V_{TO}	Threshold voltage	$T_j=125$	0.799	V
R_D	Dynamic resistance	$T_j=125$	151	m Ω
I_{DRM}	$V_D=V_{DRM}$ $V_R=V_{RRM}$	$T_j=25$	5	μA
I_{RRM}		$T_j=125$	0.2	mA

THERMAL RESISTANCES

Symbol	Parameter	Value	Unit
$R_{th(j-c)}$	junction to case (AC)	18	/W
$R_{th(j-a)}$	junction to ambient (AC)	160	/W

FIG.1: Maximum power dissipation versus RMS on-state current

FIG.2: RMS on-state current versus case temperature

FIG.7: Relative variations of gate trigger current, holding current and latching current versus junction temperature

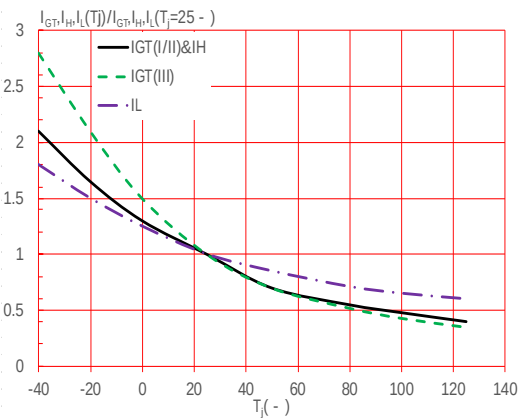
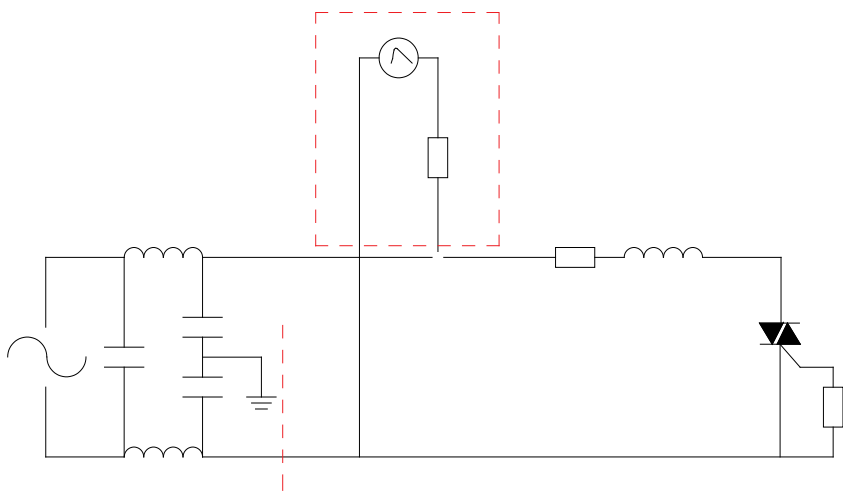


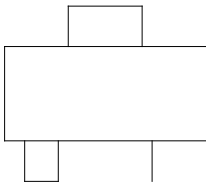
FIG.8 Test circuit for inductive and resistive loads to IEC-61000-4-5 standards



ORDERING INFORMATION

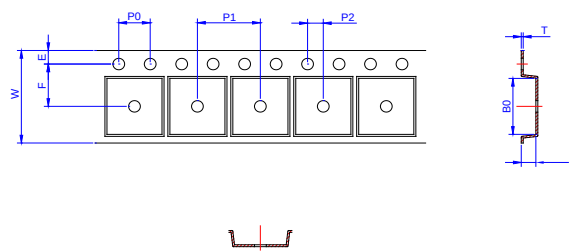
Order code	Voltage V _{DRM} /V _{RRM} (V)

PACKAGE MECHANICAL DATA



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.50	1.60	1.80	0.059	0.063	0.071
A1	0.01	0.06	0.10	0.001	0.002	0.004
B	2.90	3.00	3.10	0.114	0.118	0.122
B1	0.60	0.70	0.80	0.024	0.028	0.031
C	0.22	0.26	0.32	0.009	0.010	0.013
D	6.30	6.50	6.70	0.248	0.256	0.264
E	3.30	3.50	3.70	0.130	0.138	0.146
F	4.40			0.173		
F1	2.20			0.087		
G	0.50		1.00	0.020		0.039
H	1.50	1.75	2.00	0.059	0.069	0.079
J	6.70	7.00	7.30	0.264	0.276	0.287
K						

DELIVERY MODE



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	-		12.30	-		0.482
E	1.65	1.75	1.85	0.065	0.069	0.073
F	5.45	5.50	5.55	0.215	0.217	0.219
D0		1.55	1.60		0.061	0.063
D1		-	-			
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.95	2.00	2.05	0.077	0.079	0.081
10P0	39.80	40.00	40.20	1.567	1.575	1.583
A0	6.85	6.95	7.05	0.269	0.273	0.276
B0	7.15	7.25	7.35	0.280	0.284	0.288
K0	1.95	2.05	2.15	0.076	0.080	0.084
T	0.20	0.25	0.30	0.008	0.010	0.012

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