



JST41TE Series 41A TRIACs

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JST41TE series triacs, with high ability to withstand the shock loading of large current, provide high dv/dt rate with strong resistance to electromagnetic interface. With high commutation performances, 3 quadrants products especially recommended for use on inductive load.

Symbol	Value	Unit
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($T_j=25$ unless otherwise specified)

3 Quadrants

Symbol	Test Condition	Quadrant		Value	Unit
I_{GT}	$V_D=12V$ $R_L=33\Omega$	- -	MAX	50	mA
V_{GT}		- -	MAX	1.3	V
V_{GD}	$V_D=V_{DRM}$ $T_j=125$ R				



Symbol	Parameter		Value(MAX)	Unit
V_{TM}	$I_{TM}=60A$ $t_P=380\mu s$	$T_j=25$	1.55	V
V_{TO}	Threshold voltage	$T_j=125$	0.85	V
R_d	Dynamic resistance	$T_j=125$	9	$m\Omega$
I_{DRM}	$V_D=V_{DRM}$ $V_R=V_{RRM}$	$T_j=25$	10	μA
I_{RRM}		$T_j=125$	5	mA

Symbol	Parameter	Value	Unit
$R_{DS(on)}$	$V_{GS}=10V$ $I_{DS}=Q$		



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FIG.1 Maximum power dissipation versus RMS on-state current

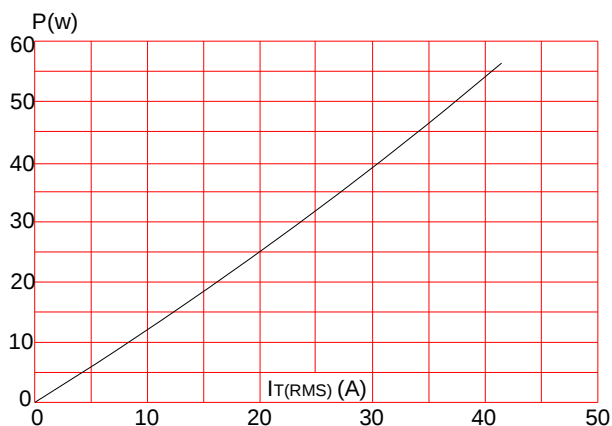


FIG.3: Surge peak on-state current versus number of cycles

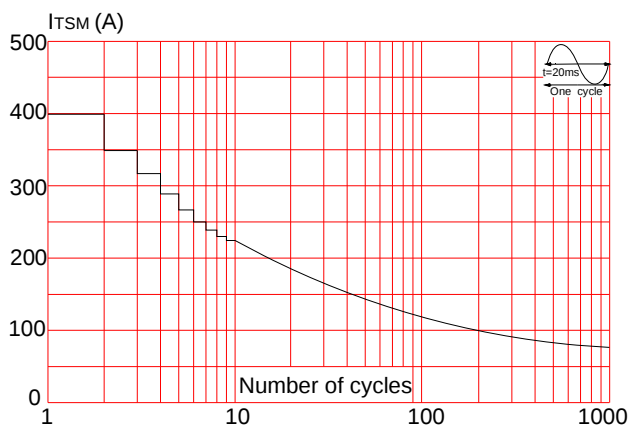


FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width $t_p < 20\text{ms}$, and corresponding value of $I^2t(dI/dt < 50\text{A}/\mu\text{s})$

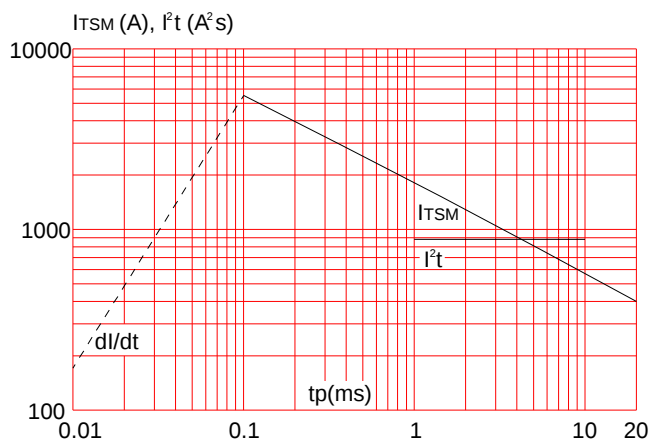


FIG.2: RMS on-state current versus case temperature

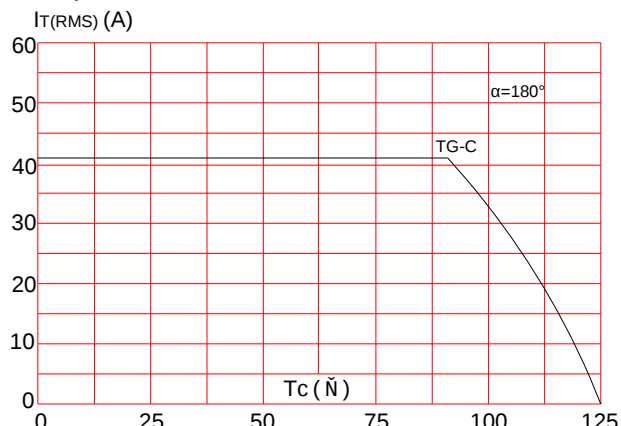


FIG.4: On-state characteristics (maximum values)

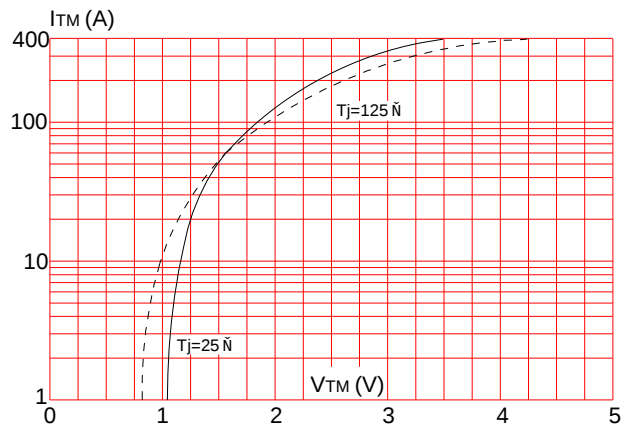
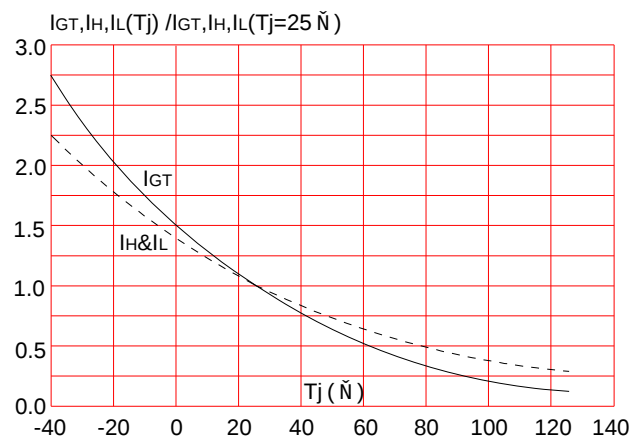


FIG.6: Relative variations of gate trigger current, holding current and latching current versus junction temperature





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